1. A digitally controlled impedance driver circuit comprising the following:

a first voltage supply that is configured to carry a first voltage during operation;

an input/output node upon which the digital controlled impedance driver circuit is to apply a signal during operation;

a first finger comprising a first field effect transistor unit having a first ideal effective length-to-width ratio and having a source terminal coupled to the first voltage supply, and further comprising a first resistor coupled in series between a drain terminal of the first field effect transistor unit and the input/output node, the first resistor having a first ideal resistance; and

a second finger comprising a second field effect transistor unit having a second ideal effective length-to-width ratio and having a source terminal coupled to the first voltage supply, wherein the second ideal effective length-to-width ratio is smaller than the first ideal effective length-to-width ratio, the second finger further including a second resistor coupled in series between a drain terminal of the second field effect transistor unit and the input/output node, the second resistor having a second ideal resistance that is smaller than the first ideal resistance.

2. A digitally controlled impedance driver circuit in accordance with Claim 1, wherein the ratio of the second ideal resistance to the first ideal resistance is between sixty percent and one hundred and fifty percent of the ratio of the second ideal effective length-to-width ratio to the first ideal effective length-to-width ratio.

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3. A digitally controlled impedance driver circuit in accordance with Claim 2, wherein the ratio of the second ideal effective length-to-width ratio to the first ideal effective length-to-width ratio is between forty percent and sixty percent.

4. A digitally controlled impedance driver circuit in accordance with Claim 2, wherein the ratio of the second ideal resistance to the first ideal resistance is between ninety percent and one hundred and ten percent of the ratio of the second ideal effective length-to-width ratio to the first ideal effective length-to-width ratio.

5. A digitally controlled impedance driver circuit in accordance with Claim 1, wherein the ratio of the second ideal effective length-to-width ratio to the first ideal effective length-to-width ratio is between forty percent and sixty percent.

6. A digitally controlled impedance driver circuit in accordance with Claim 5, further comprising the following:

a third finger comprising a third field effect transistor unit having a third ideal effective length-to-width ratio and having a source terminal coupled to the first voltage supply, wherein the third ideal effective length-to-width ratio is approximately equal to the second ideal effective length-to-width ratio, the third resistor having a third ideal resistance that is approximately equal to the second ideal resistance.

7. A digitally controlled impedance driver circuit in accordance with Claim 6, wherein the third finger further including a third resistor coupled in series between a drain terminal of the third field effect transistor unit and the input/output node.

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8. A digitally controlled impedance driver circuit in accordance with Claim 6, wherein the second transistors couples a drain terminal of the third field effect transistor unit to the input/output node.

9. A digitally controlled impedance driver circuit in accordance with Claim 6, wherein the ratio of the third ideal effective length-to-width ratio to the second ideal effective length-to-width ratio is between ninety percent and one hundred and ten percent.

10. A digitally controlled impedance driver circuit in accordance with Claim 9, wherein the ratio of the third ideal effective length-to-width ratio to the second ideal effective length-to-width ratio is one.

11. A digitally controlled impedance driver circuit in accordance with Claim 1, wherein the ratio of the second ideal effective length-to-width ratio to the first ideal effective length-to-width ratio is below forty percent.

12. A digitally controlled impedance driver circuit in accordance with Claim 11, further comprising the following:

a third finger comprising a third field effect transistor unit having a third ideal effective length-to-width ratio and having a source terminal coupled to the first voltage supply, wherein the third ideal effective length-to-width ratio is approximately equal to the second ideal effective length-to-width ratio, the third resistor having a third ideal resistance that is approximately equal to the second ideal resistance.

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13. A digitally controlled impedance driver circuit in accordance with Claim 12, wherein the third finger further including a third resistor coupled in series between a drain terminal of the third field effect transistor unit and the input/output node.

14. A digitally controlled impedance driver circuit in accordance with Claim 12, wherein the second transistors couples a drain terminal of the third field effect transistor unit to the input/output node.

15. A digitally controlled impedance driver circuit in accordance with Claim 12, wherein the ratio of the third ideal effective length-to-width ratio to the second ideal effective length-to-width ratio is between ninety percent and one hundred and ten percent.

16. A digitally controlled impedance driver circuit in accordance with Claim 15, wherein the ratio of the third ideal effective length-to-width ratio to the second ideal effective length-to-width ratio is one.

17. A digitally controlled impedance driver circuit in accordance with Claim 1, further comprising the following:

a second voltage supply that is configured to carry a second voltage during operation that is less than the first voltage, wherein the first and second field effect transistor units are respectively first and second p-type field effect transistor units;

wherein the first finger further comprises a first n-type field effect transistor unit having a source terminal coupled to the second voltage supply and a third resistor coupled in

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series between a drain terminal of the first n-type field effect transistor unit and the input/output node; and

wherein the second finger further comprises a second n-type field effect transistor unit having a source terminal coupled to the second voltage supply.

18. A digitally controlled impedance driver circuit in accordance with Claim 1, further comprising the following:

a third finger comprising a third field effect transistor unit having a third ideal effective length-to-width ratio and having a source terminal coupled to the first voltage supply, wherein the third ideal effective length-to-width ratio is approximately equal to the second ideal effective length-to-width ratio, the third resistor having a third ideal resistance that is approximately equal to the second ideal resistance.

19. A digitally controlled impedance driver circuit in accordance with Claim 18, wherein the third finger further including a third resistor coupled in series between a drain terminal of the third field effect transistor unit and the input/output node.

20. A digitally controlled impedance driver circuit in accordance with Claim 18, wherein the second transistors couples a drain terminal of the third field effect transistor unit to the input/output node.

21. A digitally controlled impedance driver circuit in accordance with Claim 18, wherein the ratio of the third ideal effective length-to-width ratio to the second ideal effective length-to-width ratio is between ninety percent and one hundred and ten percent.

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22. A digitally controlled impedance driver circuit in accordance with Claim 21, wherein the ratio of the third ideal effective length-to-width ratio to the second ideal effective length-to-width ratio is one.

23. A digitally controlled impedance driver circuit in accordance with Claim 1, wherein the first field effect transistor unit comprises a single field effect transistor.

24. A digitally controlled impedance driver circuit in accordance with Claim 1, wherein the first field effect transistor unit comprises a plurality of field effect transistor coupled in parallel between the first voltage supply and the first resistor.

25. A digitally controlled impedance driver circuit in accordance with Claim 1, wherein the digitally controlled impedance driver circuit comprises at least third, fourth, and fifth fingers, each having approximately the same impedance when turned on as the second finger, the digitally controlled impedance driver circuit further comprising the following:

a controller circuit configured during operation to periodically determine a configuration of the digitally controlled impedance driver circuit that would result in the digitally controlled impedance driver circuit approximating a target impedance;

a comparator configured to determine if the impedance of the digitally controlled impedance driver circuit should be increased or decreased; and

a noise attenuation circuit configured to turn off only one of the second, third, fourth or fifth fingers if the controller circuit determines that more impedance is needed even if

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turning off only one would not result in the configuration of the digitally controlled impedance driver circuit determined by the controller circuit.

26. A digitally controlled impedance driver circuit in accordance with Claim 25, wherein the noise attenuation circuit is further configured to turn on only one of the second, third, fourth or fifth fingers if the controller circuit determines that less impedance is needed even if turning on only one would not result in the configuration of the digitally controlled impedance driver circuit determined by the controller circuit.

27. A digitally controlled impedance driver circuit in accordance with Claim 25, wherein the controller circuit is configured to periodically make the determination of the configuration more frequently during power-up than when the digitally controlled impedance driver circuit is actually driving data to a load, and wherein the noise attenuation circuit is configured to adjust the configuration of the digitally controlled impedance driver circuit more frequently during power-up than when the digitally controlled impedance driver circuit is actually driving data to the load.

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28. A digitally controlled impedance driver circuit comprising the following:

a first voltage supply that is configured to carry a first voltage during operation;

an input/output node upon which the digital controlled impedance driver circuit is to apply a signal during operation;

a first finger comprising a first field effect transistor unit having a first effective length-to-width ratio and having a source terminal coupled to the first voltage supply, and further comprising a first resistor coupled in series between a drain terminal of the first field effect transistor unit and the input/output node, the first resistor having a first resistance; and

a second finger comprising a second field effect transistor unit having a second effective length-to-width ratio and having a source terminal coupled to the first voltage supply, the second finger further including a second resistor coupled in series between a drain terminal of the second field effect transistor unit and the input/output node, the second resistor having a second resistance,

wherein the ratio of the second effective length-to-width ratio to the first effective length-to-width ratio is less than sixty percent.

29. A digitally controlled impedance driver circuit in accordance with Claim 28, wherein the ratio of the second resistance to the first resistance is between eighty percent and one hundred and twenty percent of the ratio of the second effective length-to-width ratio to the first ideal effective length-to-width ratio.

30. A digitally controlled impedance driver circuit in accordance with Claim 28, further comprising the following:

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a third finger comprising a third field effect transistor unit having a third effective length-to-width ratio and having a source terminal coupled to the first voltage supply, wherein the third effective length-to-width ratio is approximately equal to the second effective length-to-width ratio, the third resistor having a third resistance that is approximately equal to the second resistance.

31. A digitally controlled impedance driver circuit in accordance with Claim 30, wherein the third finger further includes a third resistor coupled in series between a drain terminal of the third field effect transistor unit and the input/output node.

32. A digitally controlled impedance driver circuit in accordance with Claim 30, wherein the second transistors couples a drain terminal of the third field effect transistor unit to the input/output node.

33. A digitally controlled impedance driver circuit in accordance with Claim 30, wherein the ratio of the third effective length-to-width ratio to the second effective length-to-width ratio is between ninety percent and one hundred and ten percent.

34. A digitally controlled impedance driver circuit in accordance with Claim 28, further comprising the following:

a second voltage supply that is configured to carry a second voltage during operation that is less than the first voltage, wherein the first and second field effect transistor units are respectively first and second p-type field effect transistor units;

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wherein the first finger further comprises a first n-type field effect transistor unit having a source terminal coupled to the second voltage supply and a third resistor coupled in series between a drain terminal of the first n-type field effect transistor unit and the input/output node; and

wherein the second finger further comprises a second n-type field effect transistor unit having a source terminal coupled to the second voltage supply.

35. A digitally controlled impedance driver circuit in accordance with Claim 28, wherein the digitally controlled impedance driver circuit comprises at least third, fourth, and fifth fingers, each having approximately the same impedance when turned on as the second finger, the digitally controlled impedance driver circuit further comprising the following:

a controller circuit configured during operation to periodically determine a configuration of the digitally controlled impedance driver circuit that would result in the digitally controlled impedance driver circuit approximating a target impedance;

a comparator configured to determine if the impedance of the digitally controlled impedance driver circuit should be increased or decreased; and

a noise attenuation circuit configured to turn off only one of the second, third, fourth or fifth fingers if the controller circuit determines that more impedance is needed even if turning off only one would not result in the configuration of the digitally controlled impedance driver circuit determined by the controller circuit.

36. A digitally controlled impedance driver circuit in accordance with Claim 35, wherein the noise attenuation circuit is further configured to turn on only one of the second, third, fourth or fifth fingers if the controller circuit determines that less impedance is needed

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even if turning on only one would not result in the configuration of the digitally controlled impedance driver circuit determined by the controller circuit.

37. A digitally controlled impedance driver circuit in accordance with Claim 35, wherein the controller circuit is configured to periodically make the determination of the configuration more frequently during power-up than when the digitally controlled impedance driver circuit is actually driving data to a load, and wherein the noise attenuation circuit is configured to adjust the configuration of the digitally controlled impedance driver circuit more frequently during power-up than when the digitally controlled impedance driver circuit is actually driving data to the load.

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38. A digitally controlled impedance driver circuit comprising the following:

a first voltage supply that is configured to carry a first voltage during operation;

an input/output node upon which the digital controlled impedance driver circuit is to apply a signal during operation;

an array of fingers, each finger comprising a field effect transistor unit that is coupled between the first voltage supply and the input/output node, the field effect transistor units configured to operate in the linear region when the corresponding finger is on, and to be turned off when the finger is off;

a controller circuit configured during operation to periodically determine a configuration of the digitally controlled impedance driver circuit that would result in the digitally controlled impedance driver circuit approximating a target impedance;

a comparator configured to determine if the impedance of the digitally controlled impedance driver circuit should be increased or decreased; and

a noise attenuation circuit configured to turn off only one of the fingers if the controller circuit determines that more impedance is needed even if turning off only one finger would not result in the configuration of the digitally controlled impedance driver circuit determined by the controller circuit.

39. A digitally controlled impedance driver circuit in accordance with Claim 38, wherein the noise attenuation circuit is further configured to turn on only one of the second fingers if the controller circuit determines that less impedance is needed even if turning on only one would not result in the configuration of the digitally controlled impedance driver circuit determined by the controller circuit.

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40. A digitally controlled impedance driver circuit in accordance with Claim 38, wherein the controller circuit is configured to periodically make the determination of the configuration more frequently during power-up than when the digitally controlled impedance driver circuit is actually driving data to a load, and wherein the noise attenuation circuit is configured to adjust the configuration of the digitally controlled impedance driver circuit more frequently during power-up than when the digitally controlled impedance driver circuit is actually driving data to the load.

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